

REMARKS

In a Notice of Non-Compliant Amendment dated September 30, 2003, the amendment Applicant filed on September 17, 2003 (and received by the PTO on 9/22/03) in response to the Office Action dated June 17, 2003 was considered non-compliant for failing to meet the requirements of 37 CFR §1.121. Applicant has included canceled claims 1-90 in the claim listing in the present amendment and respectfully submits that the requirements of 37 CFR §1.21 have been met.

The present amendment is in response to the Office Action dated June 17, 2003, where the Examiner has allowed claims 111-119 and has rejected claims 91-110. By the present amendment, claims 91, 100 and 103 have been amended. Accordingly, claims 91-119 remain in the present application. Reconsideration and allowance of outstanding claims 91-110 in view of the amendments and the following remarks are respectfully requested.

A. Rejection of Claims 91-110 Under 35 USC §112, First Paragraph

The Examiner has rejected claims 91-110 under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or which it is most nearly connected, to make and/or use the invention. Applicant respectfully traverses the rejection.

Independent claim 91 specifies, among other things, “a second discrete component embedded in said single interconnect substrate.” This limitation is supported by the specification of the present application, which describes that “the internal metal layers of

substrate 102 may suitably define any number of conductive lines, printed components (e.g., inductors, transformers, capacitors, and resistors), ground planes, terminations, or the like. Embedded components (e.g., inductors, transformers, capacitors, and resistors) may also be utilized within substrate 102.” Page 7, lines 22-25 of the present application. As described in the present application, “plated or filled vias 118 function as thermal and/or electrical paths between layers of substrate 102” for this purpose. Page 7, lines 25-26 of the present application. Moreover, with reference to the unique configuration of vias according to the present invention as shown in exemplary Figure 8 of the present application, the specification notes that “blind vias 806 may be employed to route an RF signal through its shortest route to an inner layer or to form an embedded transformer.” Page 13, lines 16-17 of the present application. For these reasons, applicant respectfully submits that the present application fully supports “a second discrete component embedded in said single interconnect substrate” as specified by independent claim 91 and dependent claims 92-110. Accordingly, applicant respectfully submits that claims 91-110 meet the requirements of 35 USC §112, first paragraph.

B. Rejection of Claims 91-110 Under 35 USC §103

The Examiner has rejected claims 91-110 under 35 USC §103(a) as being unpatentable over Fukuoka (USPN 5,818,699) (“Fukuoka ‘699”) in view of Sunahara (USPN 6,153,290) (“Sunahara ‘290”). Applicant respectfully disagrees; however, in order to expedite the prosecution of the present application, applicant has amended independent claim 91. For the reasons that follow, applicant respectfully submits that

claims 91-110 are patentably distinguishable over the cited references, considered singly or in combination.

As amended, independent claim 91 specifies an integrated module comprising, among other things, “a single interconnect substrate; a first active circuit chip wire bonded to said single interconnect substrate; a second active circuit chip interconnected to said single interconnect substrate; a first ground plane integral to said interconnect substrate and operatively associated with said first active chip; and a second ground plane integral to said interconnect substrate and operatively associated with said second active chip.” This particular arrangement, also referred to in the present application as “split ground planes” significantly improves the electronic shielding and isolation between the first and second active circuit chips. See, for example, page 10, line 1 through page 11, line 14 of the present application.

In contrast, the combined disclosures of Fukuoka ‘699 and Sunahara ‘290 fail to disclose or suggest such an arrangement. For example, Fukuoka ‘699 is directed to “an approximately lead-free multi-chip module in which no lead is used mounting electronic elements and no lead is used for connecting a sealing cap.” See col. 5, lines 38-42 of Fukuoka ‘699. The various embodiments shown and described in Fukuoka ‘699 neither disclose nor suggest a “first ground plane integral to said interconnect substrate and operatively associated with said first active chip” and a separate “second ground plane integral to said interconnect substrate and operatively associated with said second active chip,” as specified by claim 91.

Furthermore, Sunahara '290 fails to cure the basic deficiencies of the Fukuoka '699. For example, Sunahara '290 is directed to a multi-layer ceramic substrate which incorporates a passive component. However, Sunahara '290 neither discloses nor suggests a "first ground plane integral to said interconnect substrate and operatively associated with said first active chip" and a separate "second ground plane integral to said interconnect substrate and operatively associated with said second active chip," as specified by claim 91. In sum, considered singly or in combination, Fukuoka '699 and Sunahara '290 fail to disclose or remotely suggest the limitations set forth in claim 91. For these reasons, applicant respectfully submits that the rejection of independent claim 91, and its corresponding dependent claims 92-110, has been overcome, and that, therefore, claims 91-110 should now be allowed.

C. **Allowed claims**


Claims 111-119 stand allowed.

D. Conclusion

For all the foregoing reasons, a Notice of Allowance directed to claims 91-119 remaining in the present application is respectfully requested.

Respectfully Submitted;
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